Abstract

A method of making byte erasable devices having elements made with nanotubes. Under one aspect of the invention, a device is made having nanotube memory elements. A structure is provided having a plurality of transistors, each with a drain and a source with a defined channel region therebetween, each transistor further including a gate over said channel. For a predefined set of transistors, a corresponding trench is formed between gates of adjacent transistors. For each trench, a defined pattern of nanotube fabric is provided over at least a horizontal portion of the structure and extending into the trench. An electrode is provided in each trench. Each defined pattern of nanotube fabric is suspended so that at least a portion is vertically suspended in spaced relation to the vertical walls of the trench and positioned so that the vertically suspended defined pattern of nanotube fabric is electromechanically deflectable into electrical communication with one of the drain and source of a transistor. An electrical communication path is provided electrically connecting each electrode so that all electrodes may electro-statically attract a corresponding defined pattern of nanotube fabric away from a transistor and toward the electrode.